

# Laboratory 3

(Due date : **002/003**: October 14<sup>th</sup>, **004**: October 15<sup>th</sup>, **005**: October 16<sup>th</sup>)

## OBJECTIVES

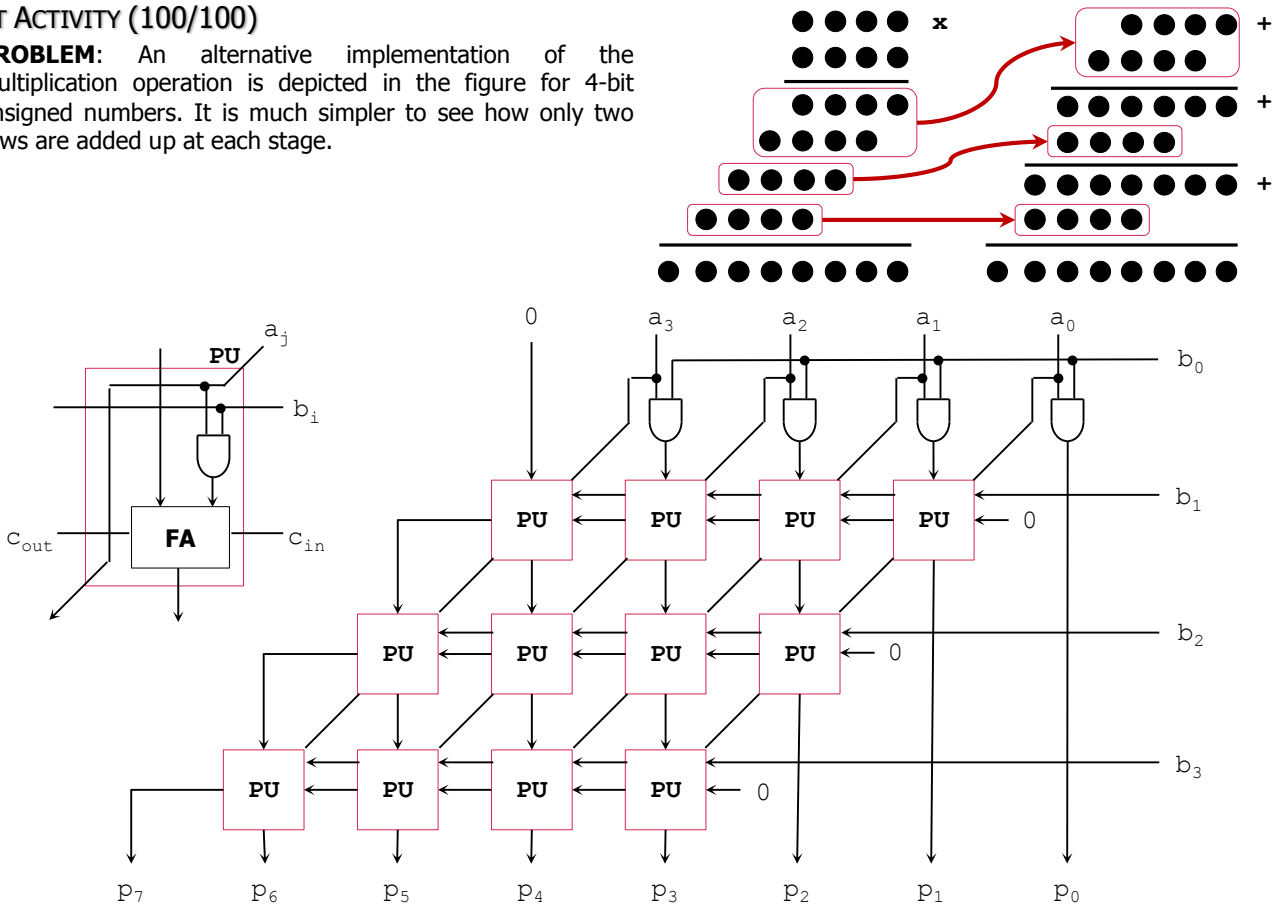
- ✓ Use the Structural Description on VHDL.
- ✓ Test arithmetic circuits on an FPGA.

## VHDL CODING

- ✓ Refer to the [Tutorial: VHDL for FPGAs](#) for a list of examples.

## FIRST ACTIVITY (100/100)

- **PROBLEM:** An alternative implementation of the multiplication operation is depicted in the figure for 4-bit unsigned numbers. It is much simpler to see how only two rows are added up at each stage.



- ✓ **NEXYS A7-50T:** Create a new Vivado Project. Select the **XC7A50T-1CSG324 Artix-7 FPGA** device.
  - ✓ Write the VHDL code for the given array multiplier of two unsigned numbers of 4 bits. Use the **Structural Description**: Create a separate file for the Full Adder, the Processing Unit (PU), and the top file (Array Multiplier).
  - ✓ Write the VHDL testbench to test the circuit for all possible cases (256 cases). Use 'for loop'.
  - ✓ Perform Functional Simulation and Timing Simulation of your design. **Demonstrate this to your TA.**
  - ✓ I/O Assignment: Create the XDC file. Nexys-4: Use SW0 to SW7 for the inputs, and LED7 to LED0 for the output.
  - ✓ Generate and download the bitstream on the FPGA and test. **Demonstrate this to your TA.**
- Submit ([as a .zip file](#)) the five generated files: VHDL code (3 files), VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

TA signature: \_\_\_\_\_

Date: \_\_\_\_\_